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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/679,000
Filing Date: October 02, 2003
Appellant(s): CHANG ET AL.

Rodney M. Anderson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 1/28/2008 appealing from the Office action mailed 4/4/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Mater

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal Identifies the ground of rejections and the associated claims under rejection to be reviewed on appeal.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,747,827	Bassett et al.	06-2004
6,651,212	Katayama et al.	11-2003
6,662,333	Zhang et al.	12-2003
6,182,239	Kramer	01-2001

(9) Grounds of Rejection

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 3-4, 6-7, 10-11, 15, 21, 23, 27-28 and 31 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 4, 3, 6, 9 and 10 of copending Application No. **10/678,893** (most recently amended on 12/19/2006), as shown in the following table. Although not all of the conflicting claims are exactly identical, they are extremely similar and are not patentably distinct from each other, as explained in the "explanation" section below.

10/679,000	**10/678,893**
1. (currently amended) A method for storing data associated with a page within a non-volatile flash memory of a memory system, the page being the smallest unit of programming in the non-volatile flash memory, and having a data area and an overhead area, the method comprising: dividing at least a part of the page into at least a first segment and a second segment; encoding data associated with the first segment according to a first error correction code (ECC) algorithm; encoding data associated with the second segment according to a second error correction code (ECC) algorithm, wherein the second segment is encoded substantially separately from the first segment; programming the page with the encoded data associated with the first and second segments.	4 (currently amended) A method for storing data within a non-volatile memory comprised of a plurality of blocks in an array formed on a semiconductor substrate, each of the plurality of blocks having an indicator indicative of whether the block is a reclaimed block, the method comprising: identifying a first block of the plurality of blocks into which the data is to be stored; responsive to the indicator associated with the first block meeting a criterion, encoding the data using a first error detection algorithm; then writing the encoded data into the first block; identifying a second block of the plurality of blocks into which data is to be stored; responsive to the indicator associated with the second block not meeting the criterion, encoding the data using a second error detection algorithm, the second error detection algorithm having a higher error detection capability than the first error detection algorithm; and then writing the encoded data into the second block.
2. The method of claim 1 wherein the first segment includes the data area and the second segment includes the overhead area.	3. The method of claim 4 wherein the first error detection algorithm is a 1-bit error detection code (ECC) algorithm and the second algorithm is a 2-bit ECC algorithm.
3. The method of claim 1 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.	9. The method of claim 6 wherein the non-volatile memory is a flash memory.
4. The method of claim 1 wherein the first ECC calculations are associated with an ECC algorithm that is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.	10. The method of claim 9 wherein the flash memory is one of a NAND flash memory and an MLC NAND flash memory.
5. The method of claim 4 wherein the first ECC algorithm is a Hamming Code ECC algorithm.	6 (previously presented). A method for storing data within a non-volatile memory, comprised a plurality of blocks in an array formed on a semiconductor substrate, of a memory

	system, the method comprising: identifying one of the plurality of blocks into which the data is to be stored; obtaining an indicator associated with the identified block, the indicator having a value indicative of a number of times the first block has been erased; determining whether the indicator is less than a threshold value, responsive to the indicator being less than the threshold value, encoding the data using the first algorithm and then writing the data encoded using a first error detection algorithm into the identified block; responsive to the indicator not being less than the threshold value, encoding the data using a second algorithm and then writing the data encoded using a second error detection algorithm into the identified block, the second error detection algorithm having a higher error detection capability than the first error detection algorithm; repeating the identifying, obtaining, determining, encoding, and writing steps for another block in the array; wherein, as a result of the repeating step, a first block in the array stores data encoded according to the first algorithm, and a second block in the array stores data encoded according to the second algorithm.
6. The method of claim 1 wherein dividing the at least part of the page into the at least two segments of the data includes: dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment.	
7. The method of claim 6 further including: performing the ECC calculations on the third segment to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.	
8. The method of claim 6 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes the overhead area.	
9. The method of claim 6 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.	
10. The method of claim 1 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.	
11. A memory system comprising: a non-volatile memory, the non-volatile memory including a page, the page having a data area and an overhead area, the data area and the overhead area being arranged to contain bits of data; code devices for	

dividing at least a part of the page into at least two segments, the at least two segments including a first segment and a second segment; code devices for performing error correction code (ECC) calculations on the first segment according to a first ECC algorithm to encode the first segment and on the second segment according to a second ECC algorithm to encode the second segment, wherein the second segment is encoded substantially separately from the first segment; and a memory area for storing the code devices.	
12. The memory system of claim 11 further including: a controller, the controller being arranged to process the code devices.	
13. The memory system of claim 11 wherein the first segment includes the data area and the second segment includes the overhead area.	
14. The memory system of claim 11 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.	
15. The memory system of claim 11 wherein the first ECC calculations are associated with an ECC algorithm that is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.	
16. The memory system of claim 15 wherein the first ECC algorithm is a Hamming Code ECC algorithm.	
17. The memory system of claim 11 wherein the code devices for dividing the at least part of the page into the at least two segments include: code devices for dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment.	
18. The memory system of claim 17 further including: code devices for performing the ECC calculations on the third segment according to one of the first and second ECC algorithm to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.	
19. The memory system of claim 17 wherein the first segment includes a first section of the data area, the third segment includes a second section of the data area, and the second segment includes the overhead area.	
20. The memory system of claim 17 wherein the	

first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.	
21. The memory system of claim 11 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.	
22. The memory system of claim 11 wherein the code devices are one of software code devices and firmware code devices.	
23. A memory system comprising: a non-volatile memory, the non-volatile memory including a page, the page having a data area and an overhead area, the data area and the overhead area being arranged to contain bits of data; means that divide at least a part of the page into at least two segments, the at least two segments including a first segment and a second segment; and means that perform error correction code (ECC) calculations on the first segment according to a first ECC algorithm to encode the first segment and on the second segment according to a second ECC algorithm to encode the second segment, wherein the second segment is encoded substantially separately from the first segment.	
24. The memory system of claim 23 wherein the first segment includes the data area and the second segment includes the overhead area.	
25. The memory system of claim 23 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.	
27. The memory system of claim 23 wherein the means that divide the at least part of the page into the at least two segments include: means that divide the page into three segments, the three segments including the first segment, the second segment, and a third segment.	
28. The memory system of claim 27 further including: means that perform the ECC calculations according to one of the first and second ECC algorithms on the third segment to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.	
29. The memory system of claim 27 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes the overhead area.	

30. The memory system of claim 27 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.	
31. The memory system of claim 23 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.	

10/679,000	10/678,893	**EXPLANATION**
1, 11 and 23	4, 6 and 9	Both describe applying a first ECC algorithm to a first segment and a second ECC algorithm to a second segment of a non-volatile flash memory; note that claims 4 and 6 of application 10/678,893 contains more limitations specifying how segment/block 1 and segment/block 2 are to be determined than application 10/679,000, thus 10/678,893 is narrower than, thus reads on, 10/679,000; also note that every non-volatile flash memory inherently has a smallest unit of programming, which may be referred to by various terms, such as page, sector, segment, block, or whatever.
3 and 15	3	Both recite a ECC algorithm that detects up to two incorrect bits and corrects up to one incorrect bit
6, 7, 27 and 28	4	Both recite the presence of a plurality of segments and the applications of ECC algorithm to each segment
10, 21 and 31	10	Both recite that the non-volatile memory is of NAND flash memory and MLC NAND flash memory

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6-9, 11-14, 17-20, 22-25 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bassett et al. (US 6,747,827, hereinafter

referred to as Bassett), and in view of Katayama et al. (US 6,651,212, hereinafter referred to as Katayama).

As to claim 1, Bassett discloses **a method for storing data associated with a page within a non-volatile flash memory of a memory system** [the corresponding "page" in Bassett's invention is a "track" of a disk memory (figure 3; column 2, lines 66-67 and column 3, lines 1-5; column 3, lines 21-25); Katayama teaches the aspect of a non-volatile flash memory disk, see below], **the page being the smallest unit of programming in the non-volatile flash memory** [every non-volatile flash memory inherently has a smallest unit of programming, which may be referred to by various terms, such as page, sector, segment, block, or whatever, since there is no standardized term in the art for "the smallest unit of programming"]**, and having a data area and an overhead area** [The radial tracks may contain magnetic states that contain information about the tracks, such as track identification data, location information, synchronization data, as well as user data (column3, lines 17-20); note that all data other than user data is overhead data]**, the method comprising**:

dividing at least a part of the page into at least a first segment and a second segment [a track is divided into a plurality of sectors (figure 3; column 2, lines 66-67 and column 3; column 4, lines 20-23)];

encoding data associated with the first segment according to a first error correction code (ECC) algorithm [For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second

type that is written to other data sectors (column 7, lines 18-23); abstract; column 6, lines 6-12; column 6, lines 39-47; column 4, lines 37-52)]; **and**

encoding data associated with the second segment according to a second error correction code (ECC) algorithm [For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23); abstract; column 6, lines 6-12; column 6, lines 39-47; column 4, lines 37-52)], **wherein the data associated with the second segment is encoded substantially separately from the data associated with the first segment** [abstract; column 3, lines 51-60; column 4, lines 37-52; column 6, lines 39-47].

Programming the page with the encoded data associated with the first and second segments [abstract; For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23)].

Regarding claim 1, the invention disclosed by Bassett is applied toward a disk memory, which is non-volatile, but Bassett does not explicitly teach that it may be a flash memory.

However, the method disclosed by Bassett et al. is equally applicable to a flash memory.

Further, Katayama et al. disclose in their invention "Recording/Reproduction device, Semiconductor memory, and Memory Card Using the Semiconductor Memory" a method of applying different ECC algorithms to different blocks of a flash memory disk [figure 1 shows the flash memory disk comprising flash memory element (115~118), on-chip ECC (120~123) and ECC circuit (107); An ECC circuit implements a first error correction using a first BCH connection code and flash memory chips implement a second error connection using a second BCH error correction code which uses the same Galois filed (abstract)].

It is further noted that both Bassett teaches that the motivation of using different ECC algorithms to different blocks of memory instead of uniformly applying the same ECC algorithm to all blocks of memory is to save memory space [reducing the number of ECC bits that need be associated with at least some of the data to be written to the disk (12), the available space on the disk for user data can be increased (abstract)].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the method disclosed by Bassett is equally applicable to a flash memory, as demonstrated by Katayama, and to incorporate the method disclosed by Bassett to a flash memory system as flash memory becomes more commonly used in the industries, as demonstrated by Katayama.

As to claim 2, Bassett teaches that **the first segment includes the data area** [the user data (The radial tracks may contain magnetic states that contain information about the tracks, such as track identification data, location information, synchronization data, as well as user data (column3, lines 17-20); note that all data other than user data

is overhead data)] **and the second segment includes the overhead area** [the overhead data includes track identification data, location information, synchronization data (The radial tracks may contain magnetic states that contain information about the tracks, such as track identification data, location information, synchronization data, as well as user data (column3, lines 17-20); note that all data other than user data is overhead data)].

As to claim 3, Bassett teaches that **the first segment includes a first section of the data area and the second segment includes a second section of the data area** [For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23); abstract].

As to claim 6, Bassett teaches that **dividing the at least part of the page into the at least two segments of the data includes**:

dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment [a track is divided into a plurality of sectors (figure 3; column 2, lines 66-67 and column 3; column 4, lines 20-23)].

As to claim 7, Bassett teaches that **performing the ECC calculations on the third segment according to one of the first and second ECC algorithms to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment** [For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written

to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23); abstract].

As to claim 8, Bassett teaches that **the first segment includes a first section of the data area, the third segment includes a second section of the data area** [For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23); abstract]**, and the second segment includes the overhead area** [the overhead data includes track identification data, location information, synchronization data (The radial tracks may contain magnetic states that contain information about the tracks, such as track identification data, location information, synchronization data, as well as user data (column3, lines 17-20); note that all data other than user data is overhead data)].

As to claim 9, Bassett teaches that **the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area** [a track is divided into a plurality of sectors (figure 3; column 2, lines 66-67 and column 3; column 4, lines 20-23); For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23); abstract].

As to claim 11, refer to "As to claim 1."

As to claim 12, Bassett teaches that **the memory system of claim 11 further including: a controller, the controller being arranged to process the code devices** [the microcontroller, figure 1, 32; figure 2; column 3, lines 39-42].

As to claim 13, refer to "As to claim 2."

As to claim 14, refer to "As to claim 3."

As to claim 17, refer to "As to claim 6."

As to claim 18, refer to "As to claim 7."

As to claim 19, refer to "As to claim 8."

As to claim 20, refer to "As to claim 9."

As to claim 22, Bassett teaches that **the code devices are one of software code devices and firmware code devices** [the ECC encoder (figure 2, 40) and the RLL encoder (figure 2, 42); column 3, lines 51-67].

As to claim 23, refer to "As to claim 1."

As to claim 24, refer to "As to claim 2."

As to claim 25, refer to "As to claim 3."

As to claim 27, refer to "As to claim 6."

As to claim 28, refer to "As to claim 7."

As to claim 29, refer to "As to claim 8."

As to claim 30, refer to "As to claim 9."

Claims 4-5, 15-16, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bassett et al. (US 6,747,827), in view of Katayama et al. (US

6,651,212, hereinafter referred to as Katayama), and further in view of Zhang et al. (US 6,662,333).

As to claim 4, Bassett in view of Katayama does not explicitly mention that **the first ECC calculations are associated with an ECC algorithm is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment**.

However, Applicants admit in the Background of the Invention Section of their disclosure that the above recited feature is well known in the art [some ECC algorithms that are used to encode and decode data for storage are known as 1-bit ECC algorithms and 2-bit ECC algorithms ... (paragraph 0009)].

Further, Zhang et al. disclose in their invention "Shared Error Correction for Memory Design" an ECC scheme in which single bit errors are corrected and double bit errors are detected [column 1, lines 24-33].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated by Applicants' admission as well as Zhang et al., hence lacking patentable significance.

As to claim 5, Bassett in view of Katayama does not explicitly mention that **the ECC Algorithm is a Hamming Code ECC Algorithm**.

However, Zhang et al. teach in their invention "Shared Error Correction for Memory Design" that Hamming Code based ECC algorithms are well known in the art [a well known error correction code is the Hamming code (column 1, lines 55-67)].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated Zhang et al., hence lacking patentable significance.

As to claim 15, refer to "As to claim 4."

As to claim 16, refer to "As to claim 5."

As to claim 26, refer to "As to claims 4-5."

Claims 10, 21 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bassett et al. (US 6,747,827), in view of Katayama et al. (US 6,651,212, hereinafter referred to as Katayama), and further in view of Kramer (US 6,182,239).

As to claims 10, 21 and 31, Bassett in view of Katayama does not mention that **the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.**

However, the inventions of Bassett are directly applicable to any type of flash memories, including NAND flash memory and MLC NAND flash memory.

Further, Kramer teaches in the invention "Fault-Tolerant Codes for Multi-Level Memories" a fault-tolerant code semiconductor flash memory storage devices including an array of individual multi-level cell (MLC) storage devices [abstract; column 2, lines 1-15] as well as NAND flash memory [column 2, lines 36-57].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this

claim is well known in the art, as demonstrated Kramer, hence lacking patentable significance.

(10) Response to Arguments

Response to Argument on double patenting rejections

Applicants contend that the provisioning double patenting rejection against Application 10/678,893 is not proper because the claims of 10/678,893 and 10/679,000 differ from one another. The Examiner disagrees with this assessment for the following reasons:

First, the following claim analysis of claim 1 of application 10/679,000 by using claims 4, 6 and 9 of application 10/678,893 as references is presented to demonstrate that all limitations recited in claim 1 of application 10/679,000 are taught by the limitations recited in claims 4, 6 and 9 of application 10/678,893:

As to claim 1 of application 10/679,000, claims 4, 6 and 9 of application 10/678,893 discloses **a method for storing data associated with a page within a non-volatile flash memory of a memory system** [**claim 4**: a method for storing data within a non-volatile memory comprising a plurality of blocks in an array; **claim 6**: a method for storing data within a non-volatile memory comprising a plurality of blocks in an array; **claim 9**: the method of claim 6 wherein the non-volatile memory is a flash memory], **the page being the smallest unit of programming in the non-volatile flash memory** [the corresponding page is the "blocks" recited in claims 4 and 6 of application 10/678,893], **and having a data area and an overhead area** [**claim 4**: a method for storing data within a non-volatile memory comprising a plurality of blocks in

an array; claim 4: each of the plurality of blocks having an indicator indicative whether the block is a reclaimed block, (note that he indicator is the corresponding overhead area); claim 6: a method for storing data within a non-volatile memory comprising a plurality of blocks in an array; **claim 6**: obtaining an indicator associated with the identified block, the indicator having a value indicative of a number of times the first block has been erased, (note that the indicator is the corresponding overhead area)], **the method comprising**:

dividing at least a part of the page into at least a first segment and a second segment [**claim 4**: identifying a first block of the plurality of blocks into which the data is to be stored, ..., identifying a second block of the plurality of blocks into which the data is to be store; (note that the first block and the second block are the corresponding first segment and the second segment, respectively); **claim 6**: identifying one of the plurality of blocks into which the data is to be stored, ..., repeating the identifying, obtaining, determining, encoding, and writing steps for another block in the array];

encoding data associated with the first segment according to a first error correction code (ECC) algorithm [**claim 4**: identifying a first block of the plurality of blocks into which the data is to be stored, responsive to the indicator associated with the first block meeting a criterion, encoding the data using a first error detection algorithm; **claim 6**: identifying one of the plurality of blocks into which the data is to be stored, responsive to the indicator being less than the threshold value, encoding the data using the first algorithm and then writing the data encoded using a first error detection algorithm into the identified block]; **and**

encoding data associated with the second segment according to a second error correction code (ECC) algorithm [**claim 4**: identifying a second block of the plurality of blocks into which the data is to be stored, responsive to the indicator associated with the second block not meeting a criterion, encoding the data using a second error detection algorithm; **claim 6**: responsive to the indicator not being less than the threshold value, encoding the data using a second algorithm and then writing the data encoded using a second error detection algorithm into the identified block, the second error detection algorithm having a higher error detection capability than the first error detection algorithm], **wherein the data associated with the second segment is encoded substantially separately from the data associated with the first segment** [**claim 4**: identifying a first block of the plurality of blocks into which the data is to be stored, responsive to the indicator associated with the first block meeting a criterion, encoding the data using a first error detection algorithm, identifying a second block of the plurality of blocks into which the data is to be stored, responsive to the indicator associated with the second block not meeting a criterion, encoding the data using a second error detection algorithm, (note that the encoding of the first block and the second block has to be done separately because different error detection algorithms are used)].

Programming the page with the encoded data associated with the first and second segments [**claim 4**: then writing the encoded data into the first block, ..., then writing the encoded data into the second block; **claim 6**: identifying one of the plurality of blocks into which the data is to be stored, responsive to the indicator being less than

the threshold value, encoding the data using the first algorithm and then writing the data encoded using a first error detection algorithm into the identified block, ..., responsive to the indicator not being less than the threshold value, encoding the data using a second algorithm and then writing the data encoded using a second error detection algorithm into the identified block, the second error detection algorithm having a higher error detection capability than the first error detection algorithm].

Thus, it is clear from the above analysis that claims 4, 6 and 9 of application 10/678,893 teach all the limitations recited in claim 1 of application 10/679,000.

Second, Examiner notices that the wording and scope of claims 4, 6 and 9 of 10/678,893 and those of claim 1 of application 10/679,000 are not exactly the same. However, the fact that the wording and scope of the claims of two applications are not exactly the same does not necessarily exclude the possibility of double patenting between the two applications. As is well known, when two claims have different scopes, the one with the narrower scope, i.e., with more limitations, would read on, hence teach, the one with the broader scope.

For example, while claim 1 of application 10/679,000 simply recites a first segment and a second segment, claim 4 of application 10/678,893 recites a first block meeting a criterion and a second block not meeting the criterion. Thus claim 4 of application 10/678,893 has the additional limitation of "meeting, or not meeting, a criterion" that is absent from claim 1 of application 10/679,000. Thus, scope of claim 4 of application 10/678,893 is narrower than that of claim 1 of application 10/679,000, and

as such, claim 4 of application 10/678,893 reads on this particular limitation recited by claim 1 of application 10/679,000.

For another example, while claim 1 of application 10/679,000 simply recites an "overhead area," claim 4 of application 10/678,893 recites "each of the plurality of blocks having an indicator indicative whether the block is a reclaimed block." Thus claim 4 of application 10/678,893 not only recites "an overhead area comprising an indicator," but also recites the additional limitation of "having an indicator indicative whether the block is a reclaimed block" that is absent from claim 1 of application 10/679,000. Thus, scope of claim 4 of application 10/678,893 is narrower than that of claim 1 of application 10/679,000, and as such, claim 4 of application 10/678,893 reads on this particular limitation recited by claim 1 of application 10/679,000.

Therefore, the provisional double patenting rejections are maintained in this Office Action.

Response to Argument on 103 rejections of claim 1 and its dependent claims

(1) Appellant argues that there is no motivation for combining the teachings from the Bassett and the Katayama references, because there is no valid reasoning to apply the teaching of the Bassett reference to a flash memory. The Examiner disagrees.

First, the inventions of both Bassett and Katayama are directed toward applying Error Correction Code (ECC) algorithms to data stored in memory in order to prevent data from corruption and to correct errors if data is corrupted.

Specifically, Bassett teaches a method applying two different ECC algorithms to data stored at different sectors/locations of a disk [A method for performing error

correction code operations on data to be read from the disk (12) of a hard disk drive (10) includes applying a first error correction code algorithm to a first set of data to be written to the hard disk drive, and a second error correction code algorithm, different from the first, to a second set of data to be written to the hard disk drive (10). The first and second error correction code algorithms may for example produce a different number of error correction code bits for application to said data. The selection between the first and second algorithms may be made, for instance, in dependence upon the physical locations (76, 78) on the disk, or in dependence upon the type of said data (80) to be written (abstract)].

Meanwhile, Katayama teaches a method applying two different ECC algorithms to data stored at a flash memory. [An ECC circuit implements a first error correction using a first BCH connection code and flash memory chips implement a second error connection using a second BCH error correction code which uses the same Galois filed (abstract)].

Thus, both inventions are closely related to each other in applying multiple ECC algorithms to stored data, and would benefit from each other's techniques to achieve a better way of applying multiple ECC algorithms to data.

Second, the ECC algorithms disclosed by both Bassett and Katayama are general ECC algorithms that are well known in the art, and can be applied to digital data regardless data is stored in a disk or stored in a flash memory. Thus, the ECC algorithms disclosed by Katayama [for example, the BCH (abstract)] can be readily applied to the disk data of Bassett, and the ECC algorithms disclosed by Bassett [for

example, as described in column 1, line 46 to column 2, line9] can be readily applied to the flash memory data of Katayama.

Third, Bassett's invention of applying different ECC algorithms to different sections of data depending on the "need" of each sector represents a more efficient and better way of applying ECC algorithms [The ECC encoder 40 may, for example, provide two or more ECC coding strategies or algorithms by which the incoming data may be encoded. The selection of which particular strategy is used may depend upon a number of factors, below described in detail, depending, for example, on the radial location on the disk at which the data is to be written, the data type, and so on (column 3, lines 54-60); it can be seen that the ability to apply a different ECC strategy to different data types could result in more efficient utilization of the disk's storage capacity (column 4, lines 44-47)].

Thus, by the same reason, the ability to apply a different ECC strategy to different data types could result in more efficient utilization of the storage capacity of the flash memory, which would be an obvious advantage that Katayama's invention can benefit because the use of the flash memory.

Thus, there is indeed a valid reason of "more efficient utilization of the storage capacity" to combine the teachings of Bassett and Katayama.

(2) Appellant further argues and discussed in great details (as shown in pages 10-12 of the Appeal Brief) that the Katayama reference fails to teach applying different ECC algorithms to different blocks of data.

First, the Examiner agrees that the Katayama reference does not teach applying different ECC algorithms to different blocks of data.

However, the Examiner only relies on the Bassett reference for teaching the limitation of "applying different ECC algorithms to different blocks of data." In fact, the Examiner presented earlier in this Office Action that Bassett teaches [For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23); abstract; column 6, lines 6-12; column 6, lines 39-47; column 4, lines 37-52)].

Thus, the Bassett reference alone teaches the limitation of "applying different ECC algorithms to different blocks of data."

Second, the Katayama reference is only relied on to teach the element of "flash memory," rather than the "disk memory" disclosed by Bassett. This is clearly stated in the claim analysis of claim 1 as presented earlier in the "Ground of Rejection" Section of this Office Action.

Thus, Appellant's argument that Katayama reference does not teach applying different ECC algorithms to different blocks of data is irrelevant, because this particular aspect is already taught by the Bassett reference. Katayama reference is merely relied on to teach that the element of "flash memory" recited in claim 1.

(3) Therefore, the Examiner's position regarding the patentability of claim 1, and all its dependent claims, remains the same as stated in the previous Office Action.

Response to Argument on 103 rejections of claim 11 and its dependent claims

Independent claim 11 recites substantially the same limitations as recited in independent claim 1, and Appellant argues again that there is no motivation for combining the teachings from the Bassett and the Katayama references, because there is no valid reasoning to apply the teaching of the Bassett reference to a flash memory; and that the Katayama reference fails to teach applying different ECC algorithms to different blocks of data.

(1) As to Appellant's argues that there is no motivation for combining the teachings from the Bassett and the Katayama references, because there is no valid reasoning to apply the teaching of the Bassett reference to a flash memory, the Examiner's response is set forth below:

First, the inventions of both Bassett and Katayama are directed toward applying Error Correction Code (ECC) algorithms to data stored in memory in order to prevent data from corruption and to correct errors if data is corrupted.

Specifically, Bassett teaches a method applying two different ECC algorithms to data stored at different sectors/locations of a disk [A method for performing error correction code operations on data to be read from the disk (12) of a hard disk drive (10) includes applying a first error correction code algorithm to a first set of data to be written to the hard disk drive, and a second error correction code algorithm, different from the first, to a second set of data to be written to the hard disk drive (10). The first and second error correction code algorithms may for example produce a different number of error correction code bits for application to said data. The selection between the first and second algorithms may be made, for instance, in dependence

upon the physical locations (76, 78) on the disk, or in dependence upon the type of said data (80) to be written (abstract)].

Meanwhile, Katayama teaches a method applying two different ECC algorithms to data stored at a flash memory [An ECC circuit implements a first error correction using a first BCH connection code and flash memory chips implement a second error connection using a second BCH error correction code which uses the same Galois filed (abstract)].

Thus, both inventions are closely related to each other in applying multiple ECC algorithms to stored data, and would benefit from each other's techniques to achieve a better way of applying multiple ECC algorithms to data.

Second, the ECC algorithms disclosed by both Bassett and Katayama are general ECC algorithms that are well known in the art, and can be applied to digital data regardless data is stored in a disk or stored in a flash memory. Thus, the ECC algorithms disclosed by Katayama [for example, the BCH (abstract)] can be readily applied to the disk data of Bassett, and the ECC algorithms disclosed by Bassett [for example, as described in column 1, line 46 to column 2, line9] can be readily applied to the flash memory data of Katayama.

Third, Bassett's invention of applying different ECC algorithms to different sections of data depending on the "need" of each sector represents a more efficient and better way of applying ECC algorithms [The ECC encoder 40 may, for example, provide two or more ECC coding strategies or algorithms by which the incoming data may be encoded. The selection of which particular strategy is used may depend upon

a number of factors, below described in detail, depending, for example, on the radial location on the disk at which the data is to be written, the data type, and so on (column 3, lines 54-60); it can be seen that the ability to apply a different ECC strategy to different data types could result in more efficient utilization of the disk's storage capacity (column 4, lines 44-47)].

Thus, by the same reason, the ability to apply a different ECC strategy to different data types could result in more efficient utilization of the storage capacity of the flash memory, which would be an obvious advantage that Katayama's invention can benefit because the use of the flash memory.

Thus, there is indeed a valid reason of "more efficient utilization of the storage capacity" to combine the teachings of Bassett and Katayama.

(2) As to Appellant's argument that the Katayama reference fails to teach applying different ECC algorithms to different blocks of data, the Examiner's response is set forth below:

First, the Examiner agrees that the Katayama reference does not teach applying different ECC algorithms to different blocks of data.

However, the Examiner only relies on the Bassett reference for teaching the limitation of "applying different ECC algorithms to different blocks of data." In fact, the Examiner presented earlier in this Office Action that Bassett teaches [For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may

be applied to data of a second type that is written to other data sectors (column 7, lines 18-23); abstract; column 6, lines 6-12; column 6, lines 39-47; column 4, lines 37-52)].

Thus, the Bassett reference alone teaches the limitation of "applying different ECC algorithms to different blocks of data."

Second, the Katayama reference is relied on to teach the element of "flash memory," rather than the "disk memory" disclosed by Bassett. This is clearly stated in the claim analysis of claim 11 as presented earlier in the "Ground of Rejection" Section of this Office Action.

Thus, Appellant's argument that Katayama reference does not teach applying different ECC algorithms to different blocks of data is irrelevant, because this particular aspect is already taught by the Bassett reference. Katayama reference is merely relied on to teach that the element of "flash memory" recited in claim 1.

(3) Therefore, the Examiner's position regarding the patentability of claim 11, and all its dependent claims, remains the same as stated in the previous Office Action.

Response to Argument on 103 rejections of claim 23 and its dependent claims

Independent claim 23 recites substantially the same limitations as recited in independent claim 1, and Appellant argues once more that there is no motivation for combining the teachings from the Bassett and the Katayama references, because there is no valid reasoning to apply the teaching of the Bassett reference to a flash memory; and that the Katayama reference fails to teach applying different ECC algorithms to different blocks of data.

(1) As to Appellant's argues that there is no motivation for combining the teachings from the Bassett and the Katayama references, because there is no valid reasoning to apply the teaching of the Bassett reference to a flash memory, the Examiner's response is set forth below:

First, the inventions of both Bassett and Katayama are directed toward applying Error Correction Code (ECC) algorithms to data stored in memory in order to prevent data from corruption and to correct errors if data is corrupted.

Specifically, Bassett teaches a method applying two different ECC algorithms to data stored at different sectors/locations of a disk [A method for performing error correction code operations on data to be read from the disk (12) of a hard disk drive (10) includes applying a first error correction code algorithm to a first set of data to be written to the hard disk drive, and a second error correction code algorithm, different from the first, to a second set of data to be written to the hard disk drive (10). The first and second error correction code algorithms may for example produce a different number of error correction code bits for application to said data. The selection between the first and second algorithms may be made, for instance, in dependence upon the physical locations (76, 78) on the disk, or in dependence upon the type of said data (80) to be written (abstract)].

Meanwhile, Katayama teaches a method applying two different ECC algorithms to data stored at a flash memory [An ECC circuit implements a first error correction using a first BCH connection code and flash memory chips implement a second error

connection using a second BCH error correction code which uses the same Galois filed (abstract)].

Thus, both inventions are closely related to each other in applying multiple ECC algorithms to stored data, and would benefit from each other's techniques to achieve a better way of applying multiple ECC algorithms to data.

Second, the ECC algorithms disclosed by both Bassett and Katayama are general ECC algorithms that are well known in the art, and can be applied to digital data regardless data is stored in a disk or stored in a flash memory. Thus, the ECC algorithms disclosed by Katayama [for example, the BCH (abstract)] can be readily applied to the disk data of Bassett, and the ECC algorithms disclosed by Bassett [for example, as described in column 1, line 46 to column 2, line9] can be readily applied to the flash memory data of Katayama.

Third, Bassett's invention of applying different ECC algorithms to different sections of data depending on the "need" of each sector represents a more efficient and better way of applying ECC algorithms [The ECC encoder 40 may, for example, provide two or more ECC coding strategies or algorithms by which the incoming data may be encoded. The selection of which particular strategy is used may depend upon a number of factors, below described in detail, depending, for example, on the radial location on the disk at which the data is to be written, the data type, and so on (column 3, lines 54-60); it can be seen that the ability to apply a different ECC strategy to different data types could result in more efficient utilization of the disk's storage capacity (column 4, lines 44-47)].

Thus, by the same reason, the ability to apply a different ECC strategy to different data types could result in more efficient utilization of the storage capacity of the flash memory, which would be an obvious advantage that Katayama's invention can benefit because the use of the flash memory.

Thus, there is indeed a valid reason of "more efficient utilization of the storage capacity" to combine the teachings of Bassett and Katayama.

(2) As to Appellant's argument that the Katayama reference fails to teach applying different ECC algorithms to different blocks of data, the Examiner's response is set forth below:

First, the Examiner agrees that the Katayama reference does not teach applying different ECC algorithms to different blocks of data.

However, the Examiner only relies on the Bassett reference for teaching the limitation of "applying different ECC algorithms to different blocks of data." In fact, the Examiner presented earlier in this Office Action that Bassett teaches [For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23); abstract; column 6, lines 6-12; column 6, lines 39-47; column 4, lines 37-52)].

Thus, the Bassett reference alone teaches the limitation of "applying different ECC algorithms to different blocks of data."

Second, the Katayama reference is relied on to teach the element of "flash memory," rather than the "disk memory" disclosed by Bassett. This is clearly stated in

the claim analysis of claim 23 as presented earlier in the "Ground of Rejection" Section of this Office Action.

Thus, Appellant's argument that Katayama reference does not teach applying different ECC algorithms to different blocks of data is irrelevant, because this particular aspect is already taught by the Bassett reference. Katayama reference is merely relied on to teach that the element of "flash memory" recited in claim 1.

(3) Therefore, the Examiner's position regarding the patentability of claim 23, and all its dependent claims, remains the same as stated in the previous Office Action.

(11) Related Proceedings Appendix

None.

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